KEITHLEY A GREATER MEASURE OF CONFIDENCE

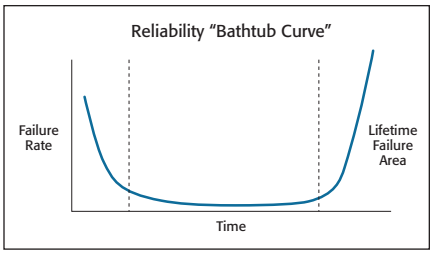

Figure 1. Typical semiconductor reliability curve.

Wafer Level Reliability Testing – A Critical Device and Process Development Step

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Changing Reliability Issues

The continuing push for more devices on a chip and faster clock speeds is driving the demand for shrinking geometries, new materials, and novel technologies. All these have a tremendous impact on the lifetime and reliability of individual devices due to increased fragility, higher power density, more complex devices, and new failure mechanisms. Processes that once produced devices with 100-year lifetimes may now yield only 10-year lifetimes – uncomfortably close to the expected operating life of systems using these devices. The smaller margin of error means that lifetime reliability must be designed in from the start and constantly monitored, from device development, through process integration, and into production; even small lifetime changes can be catastrophic to today's devices.

While reliability testing can be done at the packaged device level, many IC makers are migrating to wafer level testing for a number of reasons. Wafer level reliability (WLR) testing allows testing earlier in the process, eliminating much of the time, production capacity, money, and material lost if the packaged device fails. Turn around time is much less as a wafer can be pulled directly off the line and tested without the delay of sending the part away for packaging, which can be up to a two week process. Much of the testing is the same, allowing for relatively easy migration to wafer level testing.

Stress-measure testing is a common technique used to evaluate operating lifetimes and wear-out failure mechanisms in semiconductor devices. This testing is focused on failures on the right side of the typical failure rate bathtub curve (***Figure 1***) – i.e. failures not associated with infant mortality or manufacturing failures.

A stress-measure test is used to quickly generate curves that can be extrapolated to predict the expected operating lifetime of a device. This data is used to evaluate the device design and monitor manufacturing processes. Since typical device lifetimes are measured in years, techniques are needed to accelerate the testing. The most efficient method is to over-stress the device, measure degradation trends of key operating parameters, and extrapolate the data to the full

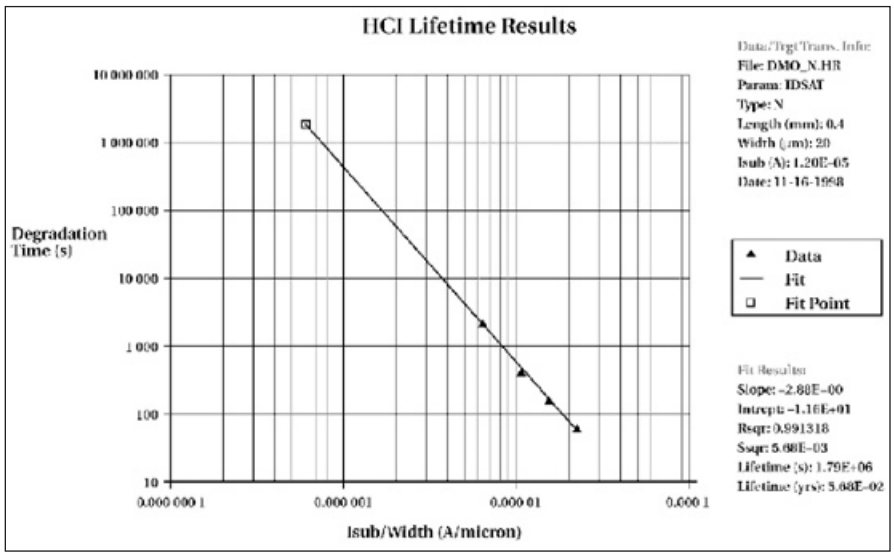

Figure 2. Example of lifetime reliability extrapolation from HCI testing.

lifetime. For example, the lower right portion (collected data) of the curve in ***Figure 2*** was generated using high stress conditions. The data generates a line that can be used to predict device lifetime under normal operating conditions (upper left portion of the curve).

Common WLR tests that use stress-measure techniques have included Hot Carrier Injection (HCI) or Channel Hot Carrier, Negative Bias Temperature Instability (NBTI), Electromigration, and Time Dependent Dielectric Breakdown (TDDB) or Charge to Breakdown (QBD). These tests have become critical in mainstream CMOS device development and process control. However, new scale factors and materials now require modifications to these established techniques, and demand instrumentation features that can implement these new techniques.

Hot Carrier Injection

HCI has been one of the key reliability tests in the last couple of CMOS generations. This is a process where high lateral electrical fields in a MOSFET generate hot carriers (high energy electrons or holes) that can damage the MOS gate oxide interface and degrade the device's I-V characteristics. This phenomenon gets worse as channel length decreases, because the lateral electric field in the channel is a function of gate voltage divided by channel length. As channel lengths have been decreasing proportionally faster than gate voltage, the increases in lateral electrical fields are causing higher energy carriers and more potential damage to the gate oxide. This damage is due to the high kinetic energy of accelerated carriers that produce electron/hole pairs through impact ionization.

Degradation will be seen in the device's I_{DS} (***Figure 3***), transconductance, and threshold voltage. Degradation first slows down the operation of the device, and will eventually cause it to stop working all together. The HCI test measures how fast a MOSFET transistor degrades when voltage stress is applied, and uses stress conditions to accelerate the degradation for quicker results that can be extrapolated to lifetime predictions under normal operating conditions (***Figure 2***).

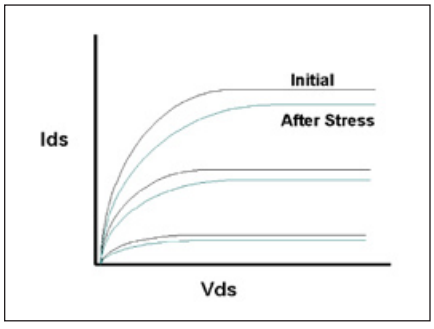

Figure 3. I-V curve showing HCI induced IDS degradation after voltage stress.

Negative Temperature Bias Instability

NBTI is a failure mode that is problematic in PMOS transistors and getting worse as threshold voltage continues to drop. NBTI degradation is measured by time dependent shifts in threshold voltages, and is associated with slower operation, more leakage, and lower drive current under negative bias stress at high temperature.

The NBTI test is typically a stress-measure sequence loop. During the stress, negative gate bias voltage is applied with the rest of transistor terminals grounded. Between two consecutive stresses, drain current is measured at normal operating condition. Degradation of drain current or threshold voltage is plotted as a function of stress time. All the stress voltages and subsequent measurements are done at high temperature (for example, 135°C).

A unique characteristic of NBTI degradation is that it can relax when stress is off. When gate voltage stress is turned off, the degradation of drain current and threshold voltage may recover and change back toward their original value. The rate of recovery is strongly dependent on temperature. At room temperature, as much as 100% recovery has been reported. If stress is resumed on the gate after recovery, the degradation will follow the previous degradation curve. At higher temperatures, there will be a portion of the degradation that is irreversible. This is called degradation lock-in.

Another aspect of the NBTI recovery problem is associated with typical transistor operation, where it is turned on and off very often. When the transistor is off, NBTI degradation may recover. Therefore, if one uses the traditional DC stress and degradation technique, there will be no recovery effect and it may underestimate the lifetime of the transistor.

One approach to handling this recovery dynamics problem is to use pulse stress instead of DC stress. In this technique the transistor is biased alternately between stress and a normal operating condition. Then degradation of threshold voltage is measured as a function of pulse frequency. This test routine provides some very important information about the nature of recovery in different applications. For example, the switching frequency is not the same for transistors in different circuits with different functionality. The frequency dependency of NBTI degradation may reveal that some part of a circuit will fail before the rest.

New Reliability Techniques

Device reliability is increasingly tied to design issues and process damage that involve the silicon (Si)/gate dielectric interface. The gate dielectric is the most sensitive part in a MOSFET. Charges inside the gate oxide and at the oxide/Si interface greatly affect transistor performance, such as when and how fast transistors turn on. Threshold voltage is directly related to the amount of charge inside the gate, and between the Si and gate interface. Damage to the oxide and interface during circuit operation is the main source of reliability problems. Channel hot carrier induced degradation, negative bias temperature instability, and charge trapping all come from the result of interface and oxide damage. Characterization of interface/oxide degradation is key to understanding those device reliability issues.

Charge Trapping in High-κ Gate Dielectrics

While high-κ material can help solve ultra-thin gate leakage problems with leading edge processes, there is no free lunch. Associated with this advantage are several technical hurdles that must be overcome. One is that the quality of the film is not very good. There are a large number of interface states as well as traps in the bulk film. The problem is when the transistor is turned on and carriers flow through the channel, some of these carriers will be trapped in the interface and bulk of the film, resulting in a shift of the threshold voltage. This charge trapping problem is reportedly more severe for NMOS than for PMOS, since electron trapping is much easier than hole trapping.

Besides looking at charge trapping dur-

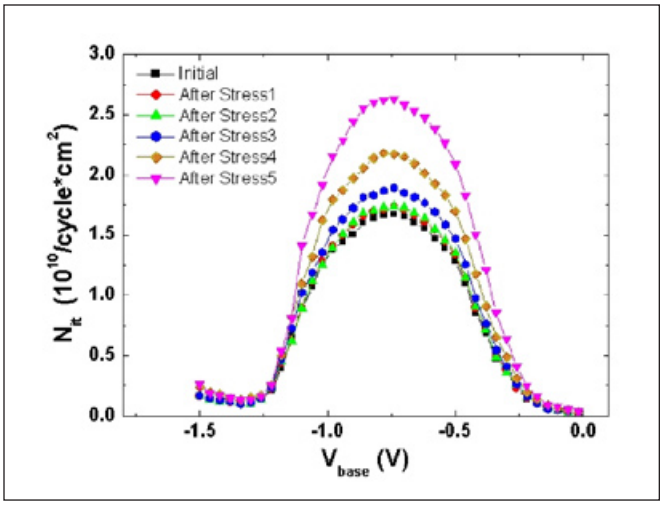

Figure 4. Formation of interface states after DC stress.

ing normal transistor operation, one can stress the gate so that charges are intentionally injected into it (charge pumping). The purpose of doing this is twofold: (1) you can control the amount of injected charge; (2) you can see if there is any interface damage due to stress and how the damage affects charge trapping behavior. The damage to the interface can be seen when measuring charge pumping current after each stress. ***Figure 4*** shows that accumulating stress creates more interface states.

Reliability Test Instrumentation Trends

As the previous text indicates, reliability tests have evolved to match the needs of new device designs and materials. While HCI is still an important reliability concern, engineers now worry about NBTI for PMOS, charge trapping for high-κ gate transistors, and cross effect between NBTI, TDDB and HCI, such as NBTI enhanced hot carrier, and TDDB enhanced NBTI. To deal with these new phenomena, measurement methodology has evolved from DC stress and measurement to a point that both DC and pulse stress are used to study degradation relaxation effect. Furthermore, instrumentation now includes more comprehensive device characterization suites, which include DC I-V, C-V, charge pumping, and charge trapping.

These evolving test requirements are challenging engineers to find the right instrumentation for efficient device and process development. The tool selected should be sensitive enough to capture all the pertinent details of parameter degradation due to stress, and flexible enough to adapt non-traditional WLR tests, such as stress C-V, charge pumping, etc. This tool should also be extendable so that one does not need to buy a completely new system every time a new test issue comes up. Finally, the tool should be easy to use so that one can focus valuable time on interpreting data, not learning to use the test system.

In terms of features, a modern reliability test stand must provide the following:

- Hardware and software that accelerates testing without compromising accuracy and extrapolated lifetimes
- Semi-auto or auto-prober with a thermal chuck
- Manipulators or a parallel probe card with low leakage
- Drivers to control instruments, probers, chucks, create tests, execute tests, and manage data
- Flexibility to accommodate user-changeable tests and stress sequences for new materials and failure mechanisms
- Analysis software that provides easy extraction of final lifetime predictions from accelerated short-term tests.

Keithley Solutions

To meet these emerging requirements, Keithley introduced the Model 4200-SCS Semiconductor Characterization System with new reliability test enhancements. Using the Model 4200-SCS, engineers can easily put different measurement techniques together to collect data in a timely fashion. This system is configurable from two to eight SMUs. The optional preamp has 0.1fA resolution. The Model 4200-SCS can also control other instruments, such as a switch matrix, C-V meter, and pulse generator without user programming. This can be done using GPIB, Ethernet, or RS-232. The interactive software has a test plan manager, interactive test setup interface, Excel-like data sheet, easy graphing capability, and more. The Model 4200's flexibility makes it an ideal characterization tool, whether it is used for development in an interactive manual mode (for single test operation) or in more automated use cases.

The Keithley Model 4200-SCS with KTEI 5.0 software makes reliability testing quick and easy. Its intuitive and point and click interface, combined with built-in test routines, makes setting up and running reliability tests as easy as getting I-V curves. The latest version of the Model 4200-SCS comes with a variety of standard stress-measure tests ready to run on boot-up, which are easily modifiable for customized testing. Its industry leading sensitivity and low-level measurement capabilities make it ideal for accurately tracking the smallest change in a degrading parameter. One feature that turns the Model 4200-SCS into an ideal reliability development station is the enhanced wafer level stress-measure loop built into the test plan manager. It includes a stress-measure loop with exit logics and a site loop for stepping through sites on a wafer. By taking advantage of these two loops, one can easily set up a customized wafer level reliability test without any programming.

Figure 5 shows the bundled HCI sample project. On the left is the sequencer showing the order of measurement tests and the overall structure of the project. The gray highlight is on the stress portion of

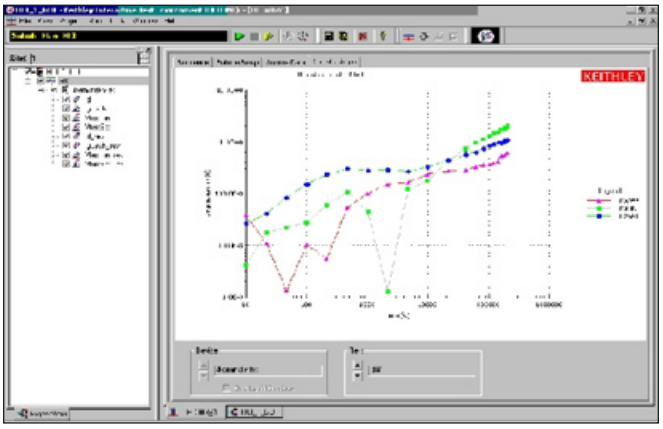

Figure 5. Model 4200-SCS HCI test screen with real-time data plots.

the sequence, where stress values, time values, and looping control are set up. Listed below the stress piece are individual tests for monitoring specific parameters. The graph shows a particular parameter being tracked over time, with each dot representing a different measure cycle after a stress cycle.

In addition, when performing traditional WLR tests such as HCI, electromigration, and TDDB/QDB, the biggest advantage of the Model 4200-SCS is that it can easily include customized WLR test routines. For example, the voltage waveform shown in Figure 6 illustrates different test modules, such as C-V, I-V and charge pumping that can be simply combined in the test plan manager for a looping sequence without programming.

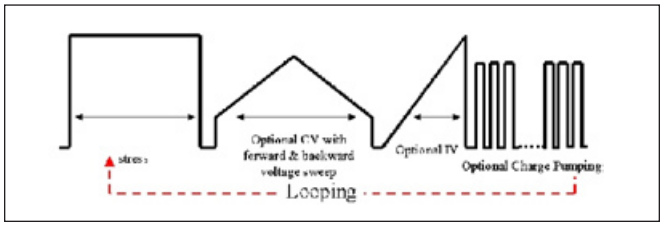

Figure 6. Customized reliability test routine incorporating different stress-measure protocols.

Another reliability system Keithley provides is the Model 4500-MTS Modular Test System. This system, built on a PCI platform, is a parallel device reliability test station for large volume testing. Its design concept is a dedicated SMU for each device under test (DUT). Since each DUT has its own SMU, the test engineer has complete freedom in assigning stress and measure conditions for each test cycle. This is especially valuable when a large sample is needed. It also eliminates the need for a switch matrix, since each DUT has dedicated system resources. A fully loaded 4500-MTS can contain up to 36 independent SMU channels.

Conclusion

Evolving design scales and new materials are making wafer level reliability testing more critical than ever. This is also driving the demand for reliability testing and modeling much further upstream – especially into the R&D process. Keithley has responded with new reliability test tools that are faster, more sensitive, and highly flexible to help drive down the cost of testing and shorten the time to market.

Additional Resources

Keithley has a variety of literature on this and related subjects. This article is based on Keithley online seminars that are a part of an on-going series conducted by Keithley engineers who are intimately involved in a variety of test and measurement techniques. To register for any of these seminars, go to www.keithley.com, click on the Events tab, and select Seminars and Conferences. Or call your local Keithley sales or support staff for more information.

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